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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,270	02/20/2002	Steven Teig	SPLX.P0127	6274
48947	7590	05/05/2005		EXAMINER
STATTLER, JOHANSEN, AND ADELI LLP				DINH, PAUL
1875 CENTURY PARK EAST SUITE 1050				
CENTURY CITY, CA 90067			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/079,270	TEIG ET AL. <i>(PM)</i>	
	<b>Examiner</b>	<b>Art Unit</b>	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 01 April 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-18 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 22 February 2002 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

**DETAILED ACTION**

- This FINAL OFFICE ACTION is a response to the remarks filed on 4/1/05.
- The remarks are not persuasive; therefore, the rejections based on prior art of record are maintained
- Claims 1-18 are pending.

***Claim Rejections - 35 USC § 103***

*The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:*

*(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scepanovic et al. (USP 6067409) in view of Rostoker et al. (USP 5822214). Scepanovic discloses a method/program comprising:

(Claims 1, 10)

- a) for a set of sub-regions that contain circuit elements (one or more of: *fig 2, 10, 15-17, 20, 26-27, 30, 33, 35, 37, 39-40, 42-48, 51-54*), identifying a connection graph (*one or more of: Steiner graph/tree in abstract, graph/tree in col 12 lines 10-20, 35-41, col 64 lines 27-28, graph/tree in fig 49-51*) during a placement operation that connects the set of sub-regions;
- b) identifying a placement cost (*i.e., col 16 lines 35-64, col 1 lines 51-57, col 2 lines 2-4, 41-45, col 3 lines 13-20, 46-46, col 7 lines 29-40, col 18 lines 3-4, col 35 lines 29-34, col 38 lines 44-66, col 47 lines 11-24, etc.*) from an attribute (*wirelength, interconnect length in col 16 lines 35-64, col 1 lines 63-65, col 2 lines 38-41, col 3 lines 13-20, col 4 lines 36-37, col 8 lines 54-63, col 9 lines 48-53, col 35 lines 29-34, col 38 lines 44-66, col 41 lines 53-58, col 42 line 67, col 47 lines 11-24, col 48 line 41, col 50 line 36, etc.*) of the connection graph, wherein the placement cost specifies a cost for the placement of the circuit elements; and
- c) using the placement cost (*col 16 lines 35-64, col 1 lines 51-57, col 2 lines 2-4, 41-45, col 3 lines 13-20, 46-46, col 7 lines 29-40, col 18 lines 3-4, col 35 lines 29-34, col 38 lines 44-66, col 47 lines 11-24*) during a placement operation to identify a placement for the circuit elements, wherein the placement specifies positions in a circuit layout for the circuit elements.

Thus Scepanovic discloses substantially all the elements in claims 1 and 10 except “*the connection graph has at least one edge that is at least partially diagonal*”

Rostoker discloses diagonal connection graph/edge in, i.e., one or more of: col 59 lines 13-65 (Steiner graph/tree for three directional routing), fig 8, 43, 73-74

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize “*connection graph has at least one edge that is at least partially diagonal*” because diagonal connection graph or diagonal routing graph reduces/shortens/minimizes routing distances, wire lengths, path lengths, interconnect paths (as taught by Rostoker in col 59 lines 13-65, col 3 lines 58-61, col 4 lines 65-67, col 6 lines 49-54, etc.) which result in the improvement/reduction/ minimizing one or more of (see Rostoker):

congestion (col 4 lines 61-67, col 6 lines 49-54, col 59 lines 13-16),

chip performance (col 2 lines 28-32),

optimizing circuit spacing and packaging (col 7 lines 1-7),

noise, layout size, and performance, line to line capacitance (col 34 lines 54-58),

minimize delay to maximize performance especially in high performance chip (col 56 line 66 to col 57 line 2),

cost (col 45 line 32+, col 59 lines 29-63)

(Claims 2, 11) wherein the attribute is a length of the graph (Scepanovic: *wirelength, interconnect length* in col 16 lines 35-64, col 1 lines 63-65, col 2 lines 38-41, col 3 lines 13-20, col 4 lines 36-37, col 8 lines 54-63, col 9 lines 48-53, col 35 lines 29-34, col 38 lines 44-66, col 41 lines 53-58, col 42 line 67, col 47 lines 11-24, col 48 line 41, col 50 line 36; also Rostoker *wirelength, interconnect length* in col 1 line 52, col 3 lines 58-61, col 4 lines 65-67 col 6 lines 49-54, etc.) and the placement cost equals the length of the connection graph (i.e., longer/higher wiring/routing length = higher cost).

(Claims 3, 12) wherein the length of the connection graph provides an estimate of a route for a routing net that is defined to include the circuit elements in the sub-regions (Scepanovic: *abstract*, col 1 lines 62-65, col 8 lines 53-63, col 9 lines 13-30, col 12 lines 18-23; also Rostoker, i.e., fig 4-5, 8, 73-78, etc)

(Claim 4, 13) wherein a net (Scepanovic: *abstract*, col 1 lines 62-65, col 8 lines 53-63, col 9 lines 13-30, col 12 lines 18-23, also Rostoker, i.e., fig 4-5, 8, 73-78, etc) is defined to include the set of circuit element in the circuit layout region, the method further comprising: before the identification of the connection graph, identifying the set of sub-regions as the set contains the circuit elements of the net

(Scepanovic: *fig 2, 10, 15-17, 20, 26-27, 30, 33, 35, 37, 39-40, 42-48, also Rostoker, i.e., fig 4-5, 8, 73-78, etc*)

(Claims 5, 14) further comprising: from storage structure (Scepanovic: system, memory, computer storage medium, apparatus (abstract/background/summary)) receiving the attribute based on the identity of the set of sub-regions

(Claims 6, 15) wherein the circuit layout region comprises a set of net (Scepanovic: *abstract, col 1 lines 62-65, col 8 lines 53-63, col 9 lines 13-30, col 12 lines 18-23 also Rostoker, i.e., fig 4-5, 8, 73-78, etc*), wherein each net includes a set of circuit element (Scepanovic: *fig 2, 10, 15-17, 20, 26-27, 30, 33, 35, 37, 39-40, 42-48, 51-54, also Rostoker, i.e., fig 4-5, 8, 73-78, etc*) the method further comprising:

for each net in the circuit layout region

(i) identifying a set of regions that contains the set of circuit elements of the net (Scepanovic: *fig 2, 10, 15-17, 20, 26-27, 30, 33, 35, 37, 39-40, 42-48, 51-54, also Rostoker, i.e., fig 4-5, 8, 73-78, etc*);

(ii) identifying a connection graph that connects the set of sub-regions (Scepanovic: *one or more of: Steiner in abstract, graph/tree in col 12 lines 10-20, 35-41, col 64 lines 27-28, fig 49-51 and/or graph/tree in col 59 lines 13-65 of Rostoker*);

(iii) identifying the length (Scepanovic: *col 16 lines 35-64, col 1 lines 63-65, col 2 lines 38-41, col 3 lines 13-20, col 4 lines 36-37, col 8 lines 54-63, col 9 lines 48-53, col 35 lines 29-34, col 38 lines 44-66, col 41 lines 53-58, col 42 line 67, col 47 lines 11-24, col 48 line 41, col 50 line 36; also Rostoker wirelength, interconnect length in col 1 line 52, col 3 lines 58-61, col 4 lines 65-67 col 6 lines 49-54, etc*) of the connection graph, wherein some connection graphs have at least one edge that is at least partially diagonal (*three directional routing graph/tree in col 59 lines 13-65 of Rostoker*)

identifying an overall placement cost from the identified length of the connection graph

(Scepanovic: *col 16 lines 35-64, col 1 lines 51-57, col 2 lines 2-4, 41-45, col 3 lines 13-20, 46-46, col 7 lines 29-40, col 18 lines 3-4, col 35 lines 29-34, col 38 lines 44-66, col 47 lines 11-24; also in col 59 lines 13-65 of Rostoker*)

(Claims 7, 16) wherein the overall placement cost quantifies the quality of an initial placement configuration (Scepanovic: *col 2 lines 10-11, col 3 lines 35-40, col 7 line 30+, col 9 line 10, col 10 lines 21-24, 58-59, col 16 line 7+, col 22 line 59, col 23 line 16, col 34 line 32+, col 39 line 1+*)

(Claims 8, 17) wherein a placer works in conjunction with a router (*place and route in Scepanovic or Rostoker*) that use a wiring model that allows routing in at least one diagonal direction (*three directional routing graph/tree in col 59 lines 13-65 of Rostoker*) wherein the an initial placement configuration is specified by a placer that does not necessarily account for potential diagonal wiring

during routing (*placing/placer does not necessarily account for wiring/routing, i.e., placing and wiring/routing are two different functions*)

(Claims 9, 18) wherein the connection graph is a Steiner Tree (*Scepanovic* (abstract) or *Rostoker* col 59 lines 13, 48, 64).

#### Response to Applicant Remarks

Particularly, the applicant states that:

“Scepanovic (main reference) does not describe a method that identifies during a placement operation, a connection graph that connects the set of sub-regions, where the connation graph has at least one edge that is at least partially diagonal as recited in claim 1” (similarly recited claim 10).

Here are examiner answers:

First, if the main reference Scepanovic disclose “*the connection graph has at least one edge that is at least partially diagonal*”; then the rejection based on Scepanovic would be a 102 rejection, not a 103 rejection.

Second, the above-mentioned prior art (Scepanovic + Rostoker) disclose all the element recited in the claims as detailed above.

Third, the issue “*the connection graph has at least one edge that is at least partially diagonal*” missing in the main reference Scepanovic is disclosed in the secondary reference Rostoker as detailed above. The motivations for use *the connection graph has at least one edge that is at least partially diagonal* are for improvement/reduction/ minimizing one or more of (see Rostoker):

congestion (col 4 lines 61-67, col 6 lines 49-54, col 59 lines 13-16),

chip performance (col 2 lines 28-32),

optimizing circuit spacing and packaging (col 7 lines 1-7),

noise, layout size, and performance, line to line capacitance (col 34 lines 54-58),

minimize delay to maximize performance especially in high performance chip (col 56 line 66 to col 57 line 2),

cost (col 45 line 32+, col 59 lines 29-63)

### Conclusion

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh  
Patent Examiner



VUTHE SIEK  
PRIMARY EXAMINER